REMARKS

Reconsideration of the application is respectfully requested.

As correctly noted by the Examiner, claim 20 depends not from claim 16 but rather from claim 18.

Turning now to the art rejections, claims 1 and 8 stand rejected as being anticipated by U.S. Patent No. 6,344,756 issued to Cecchi, et al. ("Cecchi '756"), while the rest of the claims stand rejected as being obvious in view of Cecchi '756 and other references. Applicant respectfully disagrees with the rejection, for the following reasons.

Beginning with claim 1, this claim recites an echo cancellation circuit in which a comparator has an input to receive a transmission line analog signal level. This comparator has a variable offset that is controllable, to represent a variable reference level. This comparator performs a comparison between the transmission line analog signal level and the variable reference level. To elaborate, the Specification as filed describes an echo cancellation process and apparatus that uses such a variable offset comparator, to achieve lower cost and consume less power than conventional, all digital echo cancellation methodologies. Quoting now from paragraph [0016] of the Specification as filed:

> An echo cancellation process and apparatus are described which are capable of correctly detecting far end transmitted data symbols at a near end receiver, in the presence of echo (such as near end crosstalk) due to a near end transmission. The process and apparatus may be implemented at a lower cost and perhaps consume less power than the conventional, all digital echo cancellation methodology. The process and apparatus use a variable offset comparator (i.e., VOC). According to an embodiment, the VOC has a substantially variable, digitally controllable offset and can be implemented using a standard, digital complimentary metal oxide semiconductor (i.e. CMOS) fabrication process, on the same integrated circuit chip as large scale integration logic. **Use of such a VOC (with digitally controllable offset) enables an easy calibration operation for the echo cancellation capability of an I/O circuit, to cancel inaccuracy inducing effects such as device mismatch and comparator offsets. Additionally, power consumption may be reduced in the I/O circuit as high sampling rate A/D conversion of the transmission line signal during normal operation (i.e. detection of valid, data symbols) is not required.** [Emphasis added]

In addition, the comparator may be part of a receiver that recovers the correct sequence of data symbols with improved voltage margin. Quoting now from paragraph [0021] of the Specification as filed:

> According to an embodiment of the invention, the correct sequence of data symbols may be recovered by the receiver 108 modified as shown in **Fig. 2,** with much improved voltage margin. **Fig. 2** shows an embodiment of an echo cancellation circuit that can automatically vary an implied reference level of a VOC 214, to avoid the distortion caused by echo in a received transmission line signal. **It should be noted that rather than correcting the digitized transmission line signal (by adding a correction value to each sample to literally cancel the echo distortion present in that sample), the embodiments of the invention avoid the echo distortion by shifting the implied reference level of the VOC 214 prior to translating an analog signal level into its corresponding data symbol value.** Thus, although the term 'echo cancellation' will still be used in describing the various embodiments of the invention, it should be appreciated that this is mostly for enabling a rapid understanding of the application of the invention to echo distortion problems. [Emphasis added]

Quoting now from paragraph [0025] of the Specification as filed:

> **The output of the VOC 214 provides a logic value of '0' or '1' (which, in the case of a binary communication link, may also be considered to be the received data) being a result of a comparison between the transmission line signal level and the implied, variable reference level.** An embodiment of the VOC 214 is described in U. S. Patent Application Serial No. 09/895,625 of Casper, entitled "Variable Offset Amplifier", filed on June 29, 2001 and assigned to the same assignee as that of the present application. **Fig. 7** to be described further below shows an exemplary circuit schematic of the VOC. [Emphasis added]

Finally, the offset code that is provided to the variable offset comparator may be advantageously modified by other mechanisms added to the receiver. As explained in the Specification as filed, at paragraph [0027]:

> As will be described further below, the offset code provided to the VOC 214 may be further modified by other mechanisms added to the receiver. **In such cases, the binary value at the output of the filter 226 may be added to additional binary values to form a resultant offset code that is fed to the VOC 214. An example below involves adding a binary value that represents a subtraction of an outbound wave being transmitted by the near end driver 110, where such outbound wave subtraction is useful in transmission links that accommodate simultaneous bidirectional signaling** as opposed to merely bidirectional signaling. [Emphasis added]

A point of the above presented explanation is that the use of such a variable offset comparator in an echo cancellation circuit presents substantially unexpected advantages, in contrast with traditional all digital techniques of first digitizing the input transmission line signal, and then performing an outbound wave subtraction and echo cancellation process entirely in the discrete time domain.

The Office Action indicates claim 1 is anticipated by the echo cancellation circuit of Cecchi '756 in which a **receiver** 112 has a function at its front end that subtracts a copy of the voltages produced by a local driver from the total voltages, to extract the incoming signal. The receiver 112 is not a comparator, but instead could **include** a comparator, especially, one that may perform the difference function just recited. This comparator, however, is not a variable offset comparator as recited in Applicant's claim 1.

Although Applicant is impressed with the relatively broad construction of the language in claim 1, as set forth in the Office Action, as reading on a comparison function at the front end of a receiver combined with the signal input of a driver, such a construction is not reasonably justified in view of the plain/ordinary meaning of terms such as "offset control", "comparator reference", and "driver". Although conceptually there may be a comparator at the front end of the receiver in Cecchi '756 that is fed by an output of a local driver, as part of an echo cancellation circuit, that **combination** cannot reasonably be interpreted by one skilled in the art as teaching or suggesting a variable offset comparator as recited in Applicant's claim 1.

Moreover, Applicant submits that it would have not been obvious to simply implement the comparison function with a variable offset comparator in the echo cancellation circuit of Cecchi '756. Claim 1, as amended, describes an echo cancellation circuit in which the comparator has a discrete time variable offset that is controllable, to represent the comparator's variable reference level. A driver on the same IC die as the echo cancellation circuit is to transmit driver data symbols. A discrete time echo cancellation filter has an input to receive these driver data symbols, and an output coupled to an offset control input of the comparator. Claim 1 has been amended in this manner in accordance with limitations taken from dependent 2 (now canceled).

According to the Office Action,. on pages 3-4, such would have been obvious in view of customization techniques described in the article by Lee and Razavi entitled "A 125-MHz Mixed-Signal Echo Canceller for Gigabit Ethernet on Copper Wire" ("Lee").

Even if Cecchi '756 were to explain that an echo canceller should be customized for a given physical configuration, and that an adaptive echo canceller may be used, such as described in Lee, it would not have been obvious to incorporate an echo cancellation filter whose input is to receive the driver data symbols that are transmitted by the driver, and whose output is coupled to a discrete time offset control input of the comparator, where this comparator provides a comparison between the transmission line analog signal level and a variable reference level that has been set by the offset control input. Indeed, in Cecchi '756, echo distortion is corrected by changing the slope of the replica driver whose analog output feeds a signal input of the front end comparison function in the receiver 112. This does not teach inserting a digital filter between the input of the driver and an offset control input (not an analog signal input) of a comparator.

Turning now to claim 8, this claim also stands rejected for the same reasons as claim 1. Claim 8, however, is not similar to claim 1. In claim 8, a method is recited in which a binary value is determined based on a sequence of data symbols that have been transmitted by a near end driver. This value is one that is designed to increase a voltage margin of a near end receiver, in the presence of echo. The value is applied to an offset control input of a comparator, while an analog transmission signal is applied to a signal input. The local replica driver 104 and the comparison function at the front end of the receiver 112 in Cecchi '756 cannot reasonably be viewed by one skilled in the art as teaching a comparator whose discrete time offset control input is used to receive binary values for echo cancellation in its signal input.

Turning now to claim 18, this claim has been rejected as being obvious, primarily because the differences recited in that claim from the prior art are "only found in the nonfunctional data stored in the article of manufacture". According to the Office Action at page 10, the recited echo cancellation circuit that is displayed in accordance with the instructions recited in claim 18 is "not functionally related to the substrate of the article

of manufacture", citing in support *In re Gulack*, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); and *In re Lowry*, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Applicant, however, respectfully disagrees with this interpretation of the non-patentability of printed matter.

The Federal Circuit has recently cautioned that the printed matter doctrine should not be used, particularly for computer related inventions. For example, in *In re Lowry*, the Federal Circuit held that the printed matter cases have no factual relevance where "[t]he invention as defined by the claims requires that the information be processed not by the mind but by a machine, the computer." In addition, it should be noted here that the manner in which the embodiment of the invention is described in claim 18 is not analogous to simply drawing the echo cancellation circuit on a piece of paper. What is intended for claim 18 is that a computer aided design/electronic design automation (CAD/EDA) file of the novel echo cancellation circuit be protected. The differences are not merely printed matter but actually structural limitations that appear when the recited echo cancellation circuit is simulated or manufactured, using the computer aided design/electronic design automation file. Indeed, *In re Lowry*, the Federal Circuit found that a data structure stored in memory was patentable over the prior art. In view of the forgoing, reconsideration and withdrawal of the rejection of claim 18 is respectfully requested.

Turning now to claim 13, this independent claim has been amended to incorporate the limitations of dependent claim 6 which was indicated as being allowable, together with some permissible broadening of the "bus" limitation.

Lastly, the term "substantially" has been deleted from all claims, largely because it appears to be redundant as the variable offset is stated to be controllable to represent a variable reference level for comparator.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection of the claims is improper, and how the claims are believed to be in condition for allowance. A Notice of Allowance referring to claims 1, 3-18, and 20, as amended here, is therefore respectfully requested to issue at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: February 23, 2005

By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on February 23, 2005.

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Marghux Rodriguez *February 23, 2005*